

*Remarks*

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 1-5 and 7-13 are pending in the application, with claims 1 and 11 being the independent claims. Claim 7 is canceled without prejudice or disclaimer. Claim 1 is amended to correct typographical errors and to increase its clarity. The title of the application is amended in response to the Examiner's objection. These changes introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicant respectfully requests that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

The pending claims were rejected under 35 U.S.C. 103 based on the combination of U.S. Patent 5,996,066 to Yung and U.S. Patent 6,272,514 to Petro et al. This rejection is respectfully traversed and reconsideration is requested based on the following remarks.

Yung discloses a graphics processor architecture where pixel data are "packed" into a data path. The Official Action agrees with applicant's prior comment that Yung does not teach the feature recited in claims 1 and 11 wherein "when the operands have less than the maximum number of lanes, two or more condition values are set to a same value so that each individual condition value is generated regardless of a degree of packing of the first and second source operands."

An embodiment exemplifying this feature is described at page 12 of the present specification beginning at line 13. In the disclosed embodiment, when an instruction is to be executed on a less densely packed object, all of the available condition codes are still set. For example, if there are eight condition codes available, eight condition codes

are set even if there are only one, two or four packed objects. This approach produces a significant unobvious advantage, as described in the specification. That is, once all of the condition codes have been set in this manner, they are available and can be used in subsequent instructions operating on any degree of packing.

The Petro et al. reference was cited in the Official Action as teaching grouping adjacent ALU's together for parallel operations. The Official Action asserts that it would have been obvious to modify Yung to incorporate the features of Petro et al., and that it "logically follows" that adjacent masks would be grouped in such a combination.

Applicant respectfully submits that there is no such disclosure in the references, and that the asserted combination does not make out a prima facie case of obviousness.

The Official Action asserts that the combination would be motivated by a desire to provide parallel operation in Yung. However, Yung already provides parallel operation, that is, the ability to operate on multiple pixels at one time. Petro et al. appears merely to disclose a specific logic circuit for an adder that can be partitioned like the one in Yung. The passages in Petro et al. relied upon in the Official Action thus do not appear to disclose or suggest anything relevant to the claims that is not already taught by Yung.

Further, these two references teach away from the claimed invention. While both appear to show packing data into a single register to permit faster operations, they provide and use condition codes only for the objects and object sizes actually present. Neither reference suggests, for example, setting eight condition codes when only one or two or four data elements are present. The idea of setting "extra" condition codes would require additional logic operations. This feature therefore runs counter to the specific

disclosure of Yung and Petro et al., and to their objectives of maximizing processing speed and minimizing the number of logic operations to be performed.

To make a prima facie case of obviousness, the combination of prior art must produce the features recited in the claims. Yung does not disclose the feature of generated each individual condition value even when the object is less densely packed, and neither does Petro et al. The assertion that the claimed feature would "logically follow" from such a combination is not supported by the cited references and is respectfully traversed. Neither reference discloses or suggests the above-noted advantages of the claimed invention, nor do they provide any other specific motivation for providing the claimed features.

For the reasons stated, applicants believe that on further review, the office will find that the cited references do not make out a prima facie case of obviousness. To the extent that there may be a prima facie case of obviousness based on these or other references, such case would be overcome by the unobvious advantages of the invention as described in the specification.

Thus, applicants assert that independent claims 1 and 11 are patentable over the cited references for at least these reasons. Claims 2-5, 7-10, 12 and 13, which depend therefrom, are also patentable over the cited references for at least these reasons, and further in view of their own features.

### *Conclusion*

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding objections and rejections and that they be

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withdrawn. Applicant believes that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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